178ball FBGA Specification

8Gb LPDDR3 (x32)

FEATURES

[FBGA]

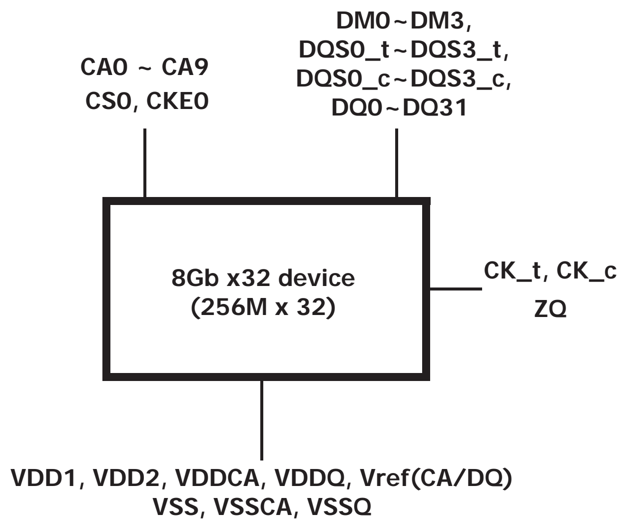
● Operation Temperature
- (-20)°C ~ 85°C

● Package
- 178-ball FBGA
- 11.0x11.5mm^2, 1.00t, 0.65mm pitch
- Lead & Halogen Free

[LPDDR3]

- VDD1 = 1.8V (1.7V to 1.95V)
- VDD2, VDDCA and VDDQ = 1.2V (1.14V to 1.30)
- HSUL_12 interface (High Speed Unterminated Logic 1.2V)
- Double data rate architecture for command, address and data Bus;
  - all control and address except CS_n, CKE latched at both rising and falling edge of the clock
  - CS_n, CKE latched at rising edge of the clock
  - two data accesses per clock cycle
- Differential clock inputs (CK_t, CK_c)
- Bi-directional differential data strobe (DQS_t, DQS_c)
  - Source synchronous data transaction aligned to bi-directional differential data strobe (DQS_t, DQS_c)
  - Data outputs aligned to the edge of the data strobe (DQS_t, DQS_c) when READ operation
  - Data inputs aligned to the center of the data strobe (DQS_t, DQS_c) when WRITE operation
- DM masks write data at the both rising and falling edge of the data strobe
- Programmable RL (Read Latency) and WL (Write Latency)
- Programmable burst length: 8
- Auto refresh and self refresh supported
- All bank auto refresh and per bank auto refresh supported
- Auto TCSR (Temperature Compensated Self Refresh)
- PASR (Partial Array Self Refresh) by Bank Mask and Segment Mask
- DS (Drive Strength)
- ZQ (Calibration)
- ODT (On Die Termination)

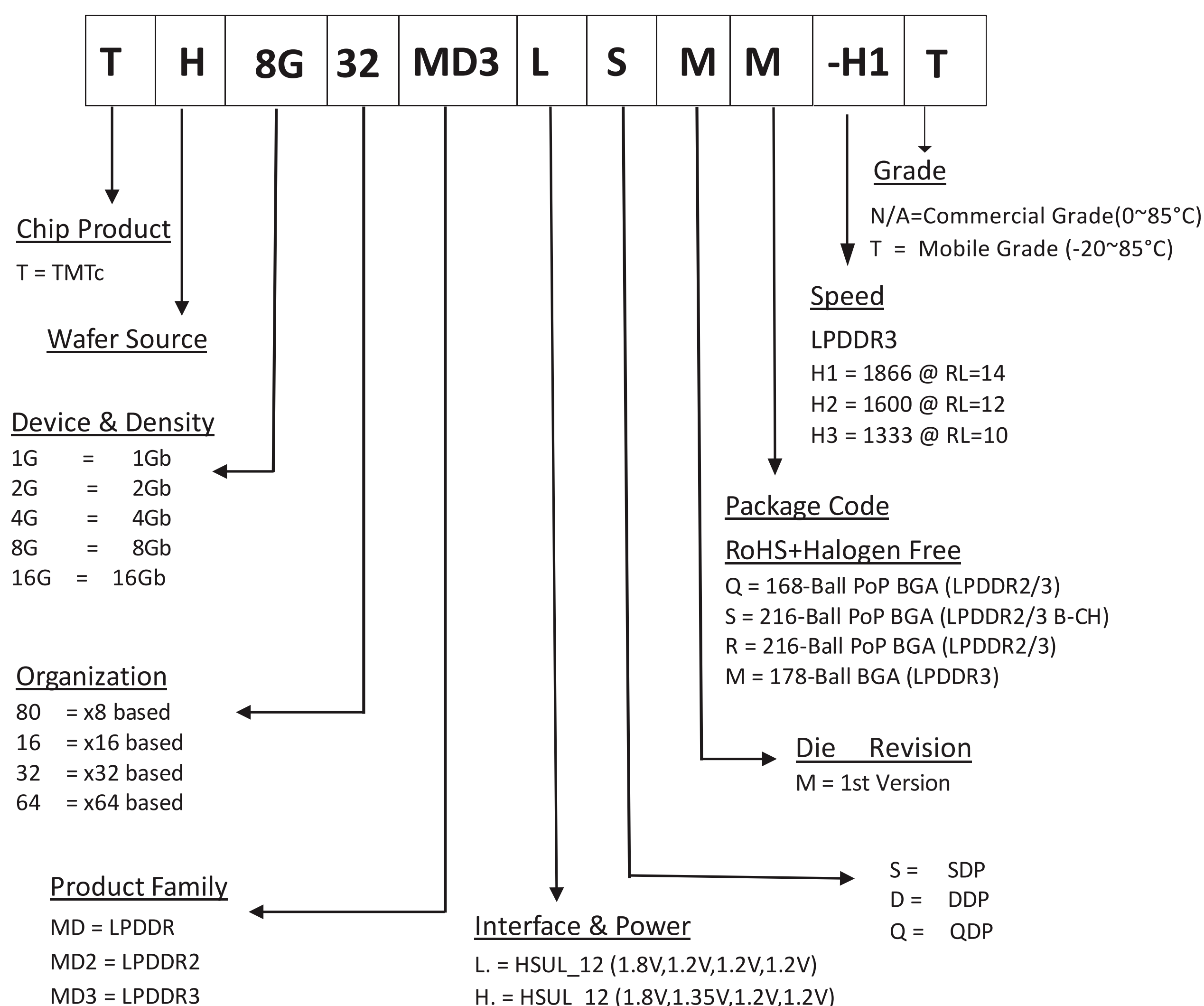
Functional Block Diagram



Note
1. Total current consumption is dependent to user operating conditions. AC and DC Characteristics shown in this specification are based on a single die. See the section of "DC Parameters and Operating Conditions"

ORDERING INFORMATION

Part Number	Memory Combination	Operation Voltage	Density	Speed	Package
TH8G32MD3LSMM-H1	LPDDR3	1.8V/1.2/1.2/1.2	8Gb(x32)	DDR3 1866	178Ball FBGA (Lead & Halogen Free)
TH8G32MD3LSMM-H2	LPDDR3	1.8V/1.2/1.2/1.2	8Gb(x32)	DDR3 1600	178Ball FBGA (Lead & Halogen Free)
TH8G32MD3LSMM-H3	LPDDR3	1.8V/1.2/1.2/1.2	8Gb(x32)	DDR3 1333	178Ball FBGA (Lead & Halogen Free)



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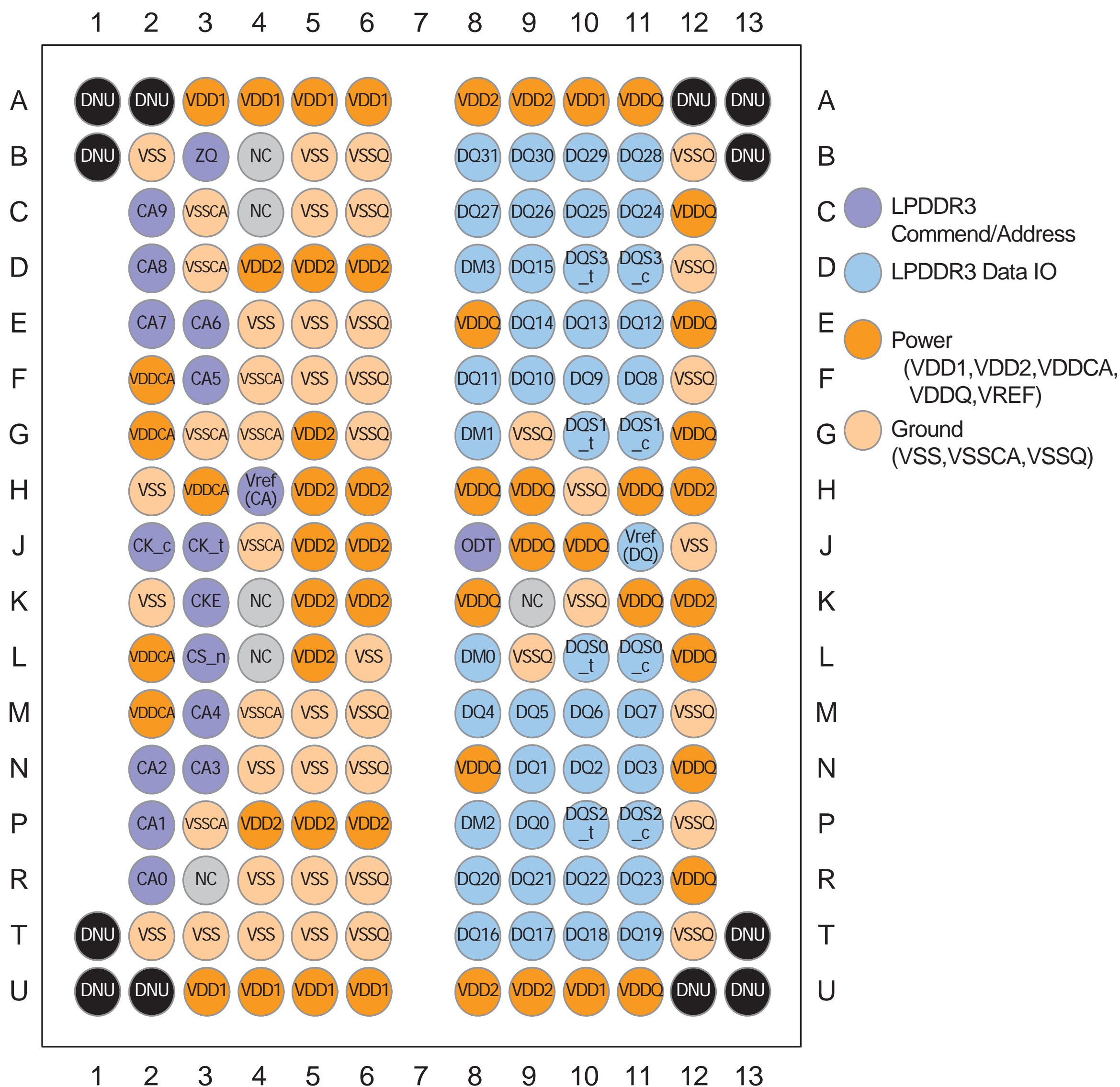
Ball ASSIGNMENT



Top View

178ball
x32 LPDDR3

Note
1. J8 will be used as "ODT". Users who don't use ODT Function can assign J8 as VSSQ.

Pin Description

SYMBOL	DESCRIPTION	Type
CS0	Chip Select	Input
CK_c, CK_t	Differential Clocks	Input
CKE0	Clock Enable	Input
CA0 ~ CA9	Command / Address	Input
DQ0 ~ DQ31	Data I/O	Input/Output
DM0 ~ DM3	Input Data Mask	Input/Output
DQS0_t ~ DQS3_t	Differential Data Strobe (rising edge)	Input/Output
DQS0_c ~ DQS3_c	Differential Data Strobe (falling edge)	Input/Output
ZQ	Drive Strength Calibration	Input/Output
VDD1	Core Power Supply	Power
VDD2	Core Power Supply	Power
VSS	Ground	Ground
VDDQ	I/O Power Supply	Power
VDDCA	CA Power Supply	Power
VSSCA	CA Ground	Ground
VSSQ	I/O Ground	Ground
VREF	Reference Voltage	Power
ODT	On Die Termination Enable	Input

Input/Output Capacitance

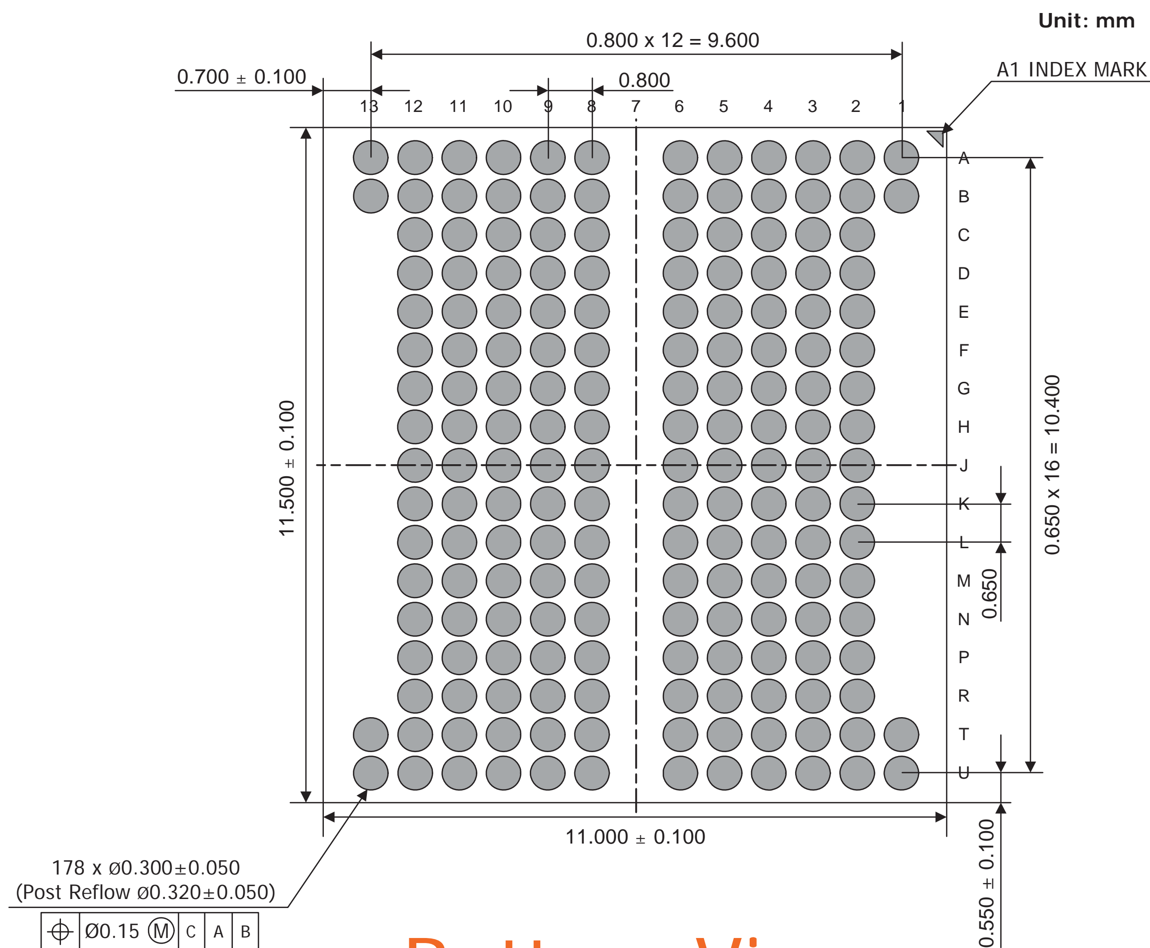
Parameter	Symbol	Min	Max	Unit
Input capacitance, CK_t and CK_c	CCK	TBD	TBD	pF
Input capacitance, all other input-only pins	CI	TBD	TBD	pF
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	TBD	TBD	pF
Input/Output Capacitance ZQ	CZQ	TBD	TBD	pF

(TOPER; VDDQ = 1.14-1.3V; VDDCA = 1.14-1.3V; VDD1 = 1.7-1.95V, VDD2 = 1.14-1.3V)

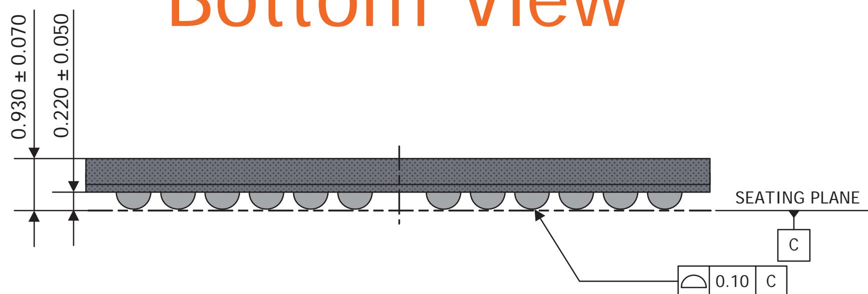
Note:
1. This parameter applies to both die and package.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSCA, VSSQ applied and all other pins floating).
3. CI applies to CS_n, CKE, CA0-CA9.
4. DM loading matches DQ and DQS.
5. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)
6. Maximum external load capacitance on ZQ pin, including packaging, board, pin, resistor, and other LPDDR3 devices: 5pF.

PACKAGE INFORMATION

178 Ball 0.65mm pitch 11.0mm x 11.5mm [t = 1.00mm max] FBGA



Bottom View



Front View

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8Gb LPDDR3 SDRAM